Designers' Forum

The Designers'Forum is conceived as a unique program that shares the design experience and solutions of real product developments among LSI designers and EDA tool providers. The topics discussed in this forum include:

Oral Sessions:

(4A) Trends in EDA
- The golden age of EDA — clock design, machine learning and A-I collaboration, Zhuo Li, Cadence
- New Trend on High-Level Synthesis and Customized Compiler for Edge Intelligence, Deming Chen, UIUC
- Data-driven Instant Model Synthesis Enhanced by Learning Algorithms For DTCO Enablement In the FinFET Era, Yanfeng li, Platform DA

(6D) Emerging Design
- Recent advances in hardware security and testing tools, Junfeng Fan, OSR
- Design of energy-efficient dynamic reconfigurable cryptographic chip, Jinjiang Yang, Tsinghua
- Cognitive SSD controller: A case for agile domain-specific SoC design, Ying Wang, ICT

(9D) AI Accelerators
- AI chips, what's next: architecture, tools, and methodology, Shan Tang
- Computing-in-memory SoC chip for neural network inference, Shaodi Wang, Witin Tech
- GAN in industry practices, Dong Wang, VisualDeep

Session 4A (10:15-11:30, Jan. 15th)

[**Trends in EDA**]

The purpose of this session is to share and discuss recent advancements and trends in the EDA field. The first talk highlights some new trends and challenges in EDA design and discusses academic and industry collaboration during this new age. The second presentation discusses how to implement Edge intelligence with domain-specific high-level synthesis tools. The third talk presents a complete device modeling system with super-fast device characterization capability based on learning algorithms.

Session 6D (15:45-17:00, Jan. 15th)

[Emerging Design]

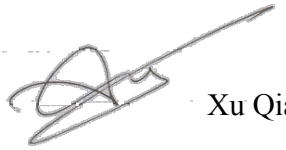
The purpose of this session is to share latest LSI designs and design methodologies. The first talk presents leading industry equipment and tools on security test. The second presentation introduces a coarse-grained dynamic reconfigurable cryptographic chip for high-throughput secure network processing and cloud computing. The third talk presents a case study on the so-called Cognitive SSD controller, a flexible and energy-efficient solution to unstructured data analysis.

Session 9D (15:45-17:00, Jan. 16th)

[AI accelerators]

The purpose of this session is to share and discuss latest advancements in AI accelerators. The first talk gives a visionary perspective on how the future AI chips will be designed, as the first generation of AI chips is getting mature. The second presentation introduces edge neural processing chips with analog computing-in-memory technology simultaneous achieving low-power, high-performance, and low-cost. The third talk discusses how generative adversarial networks are used in practice in fashion-related industries.

Designers' Forum Chair:



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