Best Paper Award

Award Winners

2D-1: "Equivalent Capacitance Guided Dummy Fill Insertion for Timing and Manufacturability"
Sheng-Jung Yu, Chen-Chien Kao, Chia-Han Huang, Iris Hui-Ru Jiang (National Taiwan Univ., Taiwan)

7B-3 : "Towards Area-Efficient Optical Neural Networks: An FFT-based Architecture"
Jiaqi Gu, Zheng Zhao, Chenghao Feng, Mingjie Liu, Ray T. Chen, David Z. Pan (Univ. of Texas, Austin, USA)

Candidates

1C-1: "Integrated Airgap Insertion and Layer Reassignment for Circuit Timing Optimization"
*Younggwang Jung, Daijoon Hyun, Youngsoo Shin (KAIST,Republic of Korea)

1D-1: "Analyzing The Security of The Cache Side Channel Defences With Attack Graphs"
*Limin Wang, Ziyuan Zhu, Zhanpeng Wang, Dan Meng (Chinese Academy of Sciences, China)

2B-1: "Co-Exploring Neural Architecture and Network-on-Chip Design for Real-Time Artificial Intelligence"
Lei Yang (Univ. of Pittsburgh, USA), Weiwen Jiang (Univ. of Notre Dame, USA), Weichen Liu (Nanyang Technological Univ., Singapore), Edwin Sha (East China Normal Univ., China), Yiyu Shi (Univ. of Notre Dame, USA), Jingtong Hu (Univ. of Pittsburgh, USA)

2D-1: "Equivalent Capacitance Guided Dummy Fill Insertion for Timing and Manufacturability"
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3C-1: "S3 DET: Detecting System Symmetry Constraints for Analog Circuits with Graph Similarity"
Mingjie Liu, Wuxi Li, Keren Zhu, Biying Xu, *Yibo Lin, Linxiao Shen, Xiyuan Tang, Nan Sun, David Z. Pan(Univ. of Texas, Austin, USA)

5A-1: "Towards Design Methodology of Efficient Fast Algorithms for Accelerating Generative Adversarial Networks on FPGAs"
Jung-Woo Chang, *Saehyun Ahn, Keon-Woo Kang, Suk-Ju Kang (Sogang Univ., Republic of Korea)

5B-1: "Towards Read-Intensive Key-Value Stores with Tidal Structure Based on LSM-Tree"
Yi Wang, Shangyu Wu, Rui Mao (Shenzhen Univ., China)

5C-1: "Unified Redistribution Layer Routing for 2.5D IC Packages"
Chun-Han Chiang, *Fu-Yu Chuang, Yao-Wen Chang (National Taiwan Univ., Taiwan)

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Jiaqi Gu, Zheng Zhao, Chenghao Feng, Mingjie Liu, Ray T. Chen, David Z. Pan (Univ. of Texas, Austin, USA)

8B-1: "Reliability-Oriented IEEE Std. 1687 Network Design and Block-Aware High-Level Synthesis for MEDA Biochips"
Zhanwei Zhong, Tung-Che Liang, *Krishnendu Chakrabarty (Duke Univ., USA)

8C-1: "Modulo Scheduling with Rational Initiation Intervals in Custom Hardware Design"
*Patrick Sittel (Univ. of Kassel, Germany), John Wickerson (Imperial College London, UK), Martin Kumm (Univ. of Applied Sciences Fulda, Germany), Peter Zipf (Univ. of Kassel, Germany)

8D-1: "WEID: Worst-Case Error Improvement in Approximate Dividers"
*Hassaan Saadat (Univ. of New South Wales, Sydney, Australia), Haris Javaid (Xilinx, Singapore), Aleksandar Ignjatovic, Sri Parameswaran (Univ. of New South Wales, Sydney, Australia)