Design of a Single-Stage Wireless Charger with 92.3%-Peak-Efficiency for Portable Devices Applications

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Abstract – This summary presents a fully-integrated wireless charger to achieve high efficiency with low cost and volume. The charger realizes power rectification, voltage regulation and CC-CV charging in one power stage only. A bootstrapping technique is also designed for on-chip integration of the bootstrap capacitors. A chip prototype was fabricated in a standard 0.35μm CMOS process with a die area of 8mm². The charger achieves peak efficiency of 92.3% and 91.4% when the charging currents are 1A and 1.5A, respectively.

I. Introduction

Wireless charging provides a convenient and reliable way to charge batteries of electronic devices. High-efficiency low-cost wireless power receivers with regulated output voltages are designed recently [1], [2]. However, it still needs an extra battery charger to implement standard CC (constant current) and CV (constant voltage) charging profiles [3]. Fig. 1 shows a conventional wireless charger with three power processing stages (power rectification, voltage regulation and CC-CV charging) [2], [3], and an improved two-stage scheme that integrates power rectification and voltage regulation into one stage [1] to improve efficiency and reduce cost. Wireless chargers using one power stage only are presented in [4]–[6]. A resonant current-mode approach is proposed in [4] to charge the battery from the resonant tank directly without rectification and regulation, and the maximum available current from the rectifier is used to charge the battery in [5] [6]. However, CC-CV charging cannot be implemented in these chargers. In this summary [8], a fully integrated single-stage wireless charger with CC-CV charging is presented. Power rectification, voltage regulation and CC-CV charging are achieved in a single power stage to improve the efficiency and to reduce the cost and volume of the charger.

II. Proposed Single-Stage Wireless Charger

Fig. 2 shows the block diagram of the charger [8] that consists of a CC-CV charging controller and a fully-integrated power stage. The power stage with 4 NMOS on-chip switches ($M_{LS1,2}$ and $M_{HS1,2}$) can be configured into 1X mode, ½X mode and 0X mode as introduced in [1]. The charger has CC mode and CV mode, and the charging mode is determined by comparing the feedback voltage V_{fb} with the reference voltage V_{ref} using a hysteresis comparator CMP_H. When the battery voltage V_{bat}<4.2V, the charger works in the CC mode. The charging current I_{ch} is regulated to a pre-defined value by the CC loop, and V_{bat} is charged up gradually. When V_{bat} reaches 4.2V the charger is switched to the CV mode, and the CV loop takes over the control to regulate V_{bat} at 4.2V until charging is completed (I_{ch}=0). Both the CC loop and the CV loop use the 3-mode operation to achieve regulation [1], and they are designed to share the same PWM controller and V_{ref} for smooth transition from the CC mode to the CV mode.

Fig. 3 shows the schematic and working principle of the current sensing and estimation circuit. When the power stage works in 1X mode, ½X mode and 0X mode, the output current is equal to $2I_{ac½}$, $I_{ac½}$ and 0, respectively. I_{ch} is then given by

$$I_{ch} = \begin{cases} I_{ac½} + I_{ac½} \times \overline{D_{PWM}} & (S_{Mode} = 0) \\ I_{ac½} \times D_{PWM} & (S_{Mode} = 1) \end{cases}$$

where D_{PWM} is the duty ratio of the PWM controller. Hence, I_{ch} can be estimated by using D_{PWM} and sensing $I_{ac½}$. As shown in Fig. 3, I_{ac1} is first sensed by scaling down the current flowing through M_{LS1} and further be averaged by a low pass filter. Then, S_{Mode} and D_{PWM} are used to control switches $S_{1,2}$ to estimate I_{ch}. Therefore, no sensing resistor is added to degrade the efficiency. To further improve the sensing accuracy, the off-delay compensation technique [7] is used to eliminate the reverse current of I_{ac1}.

In this design, NMOS transistors are employed to implement the high-side power transistors $M_{hs1,2}$ to reduce conduction loss, and an on-chip bootstrapping technique is further designed to reduce the sizes of the bootstrapping capacitors ($C_{boot1,2}$) for on-chip integration. As shown in Fig. 4, $C_{boot1,2}$ are pre-charged to 5V alternately by a single-input-dual-output voltage doubler and then left to be discharged to 3V before and after turning on $M_{hs1,2}$. The voltage doubler has 16 phases, and adaptive phase control is introduced to determine the number of active phases based on the voltage level of V_{bat} to prevent $C_{boot1,2}$ from being over-charged.

III. Measurement Results

The charger was fabricated in a 0.35 μm CMOS process. Fig. 5 shows the chip micrograph with a die area of 8 mm². Fig. 6 shows the testing setup. Fig. 7 shows the measured waveforms of $V_{ac1,2}$ and $V_{Cboot1,2}$ (=$V_{boot1,2}$−$V_{ac1,2}$) when V_{bat} is 2.8V and 4V, respectively. I_{ch} is regulated by switching the power stage between 1X mode and ½X mode. Fig. 7 also demonstrates the effectiveness of the on-chip bootstrapping technique, it can be observed that $C_{boot1,2}$ are charged to 5V alternately to properly turn on $M_{hs1,2}$. As shown in Fig. 8, thanks to the single-stage topology with all-NMOS power transistors, the peak efficiency of the charger reaches 92.3% and 91.4% when I_{ch} is 1A and 1.5A, respectively. Moreover, the efficiency of the charger is higher than 88.1% and 86.5% in the entire CC mode, respectively.

The measured waveforms of I_{ch}, V_{bat} and $V_{ac1,2}$ during a completed charging process are shown in Fig. 9. It takes around 10ms for the charger to charge 2x4.7mF capacitors from 2.8V to 4.2V with 1A I_{ch}. CC-CV charging profile is successfully implemented with a smooth transition from CC mode to CV mode. The performance comparison with state-of-the-art wireless chargers is given in Table I. The presented charger is the only work that achieves power rectification, voltage regulation and CC-CV charging in a single power stage.

References

[1] L. Cheng, et al., "A 6.78-MHz single-stage wireless power receiver using a 3-mode reconfigurable resonant regulating rectifier," *JSSC*, vol. 52, no. 5, pp.

978-1-7281-4123-7/20/$31.00 ©2020 IEEE

1412–1423, May 2017.

[2] J. T. Hwang, et al., "An all-in-one (Qi, PMA and A4WP) 2.5W fully integrated wireless battery charger IC for wearable applications," *ISSCC*, Jan. 2016, pp. 378–380.

[3] Y. Wang, et al., "A 13.56MHz wireless power and data transfer receiver achieving 75.4% effective-power-conversion efficiency with 0.1% ASK modulation depth and 9.2mW output power," *ISSCC*, Feb. 2018, pp. 142–144.

[4] M. Choi, et al., "A current-mode wireless power receiver with optimal resonant cycle tracking for implantable systems," *ISSCC*, pp. 372–373, Feb. 2017.

[5] M. Huang, et al., "A reconfigurable bidirectional wireless power transceiver with maximum-current charging mode and 58.6% battery-to-battery efficiency," *ISSCC*, pp.376–377, Feb. 2017.

[6] F. Mao, et al., "A reconfigurable cross-connected wireless-power transceiver for bidirectional device-to-device charging with 78.1% total efficiency," *ISSCC*, pp. 140–142, Feb. 2018..

[7] L. Cheng, et al., "Adaptive on/off delay-compensated active rectifiers for wireless power transfer systems," *JSSC*, vol. 51, no. 3, pp. 712–723, Mar. 2016.

[8] L. Cheng, et al., "A 6.78MHz 92.3%-peak-efficiency single-stage wireless charger with CC-CV charging and on-chip bootstrapping techniques," *VLSIC*, Jun. 2019, pp. C320–C321.

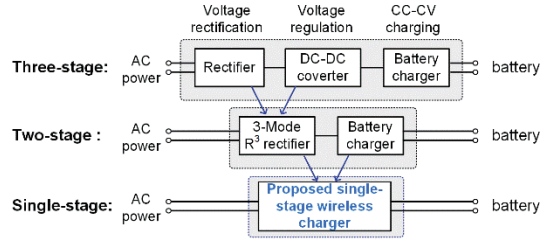

Fig. 1 Topologies of wireless chargers [8].

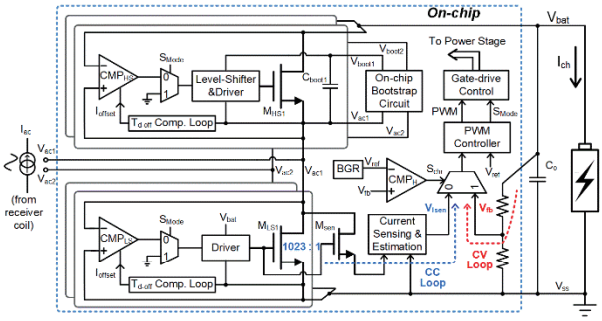

Fig. 2 Block diagram of the designed single-stage wireless charger [8].

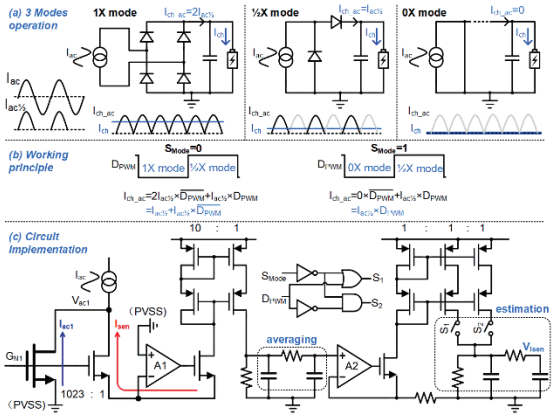

Fig. 3 Schematic and working principle of the current sensing and estimation circuit [8].

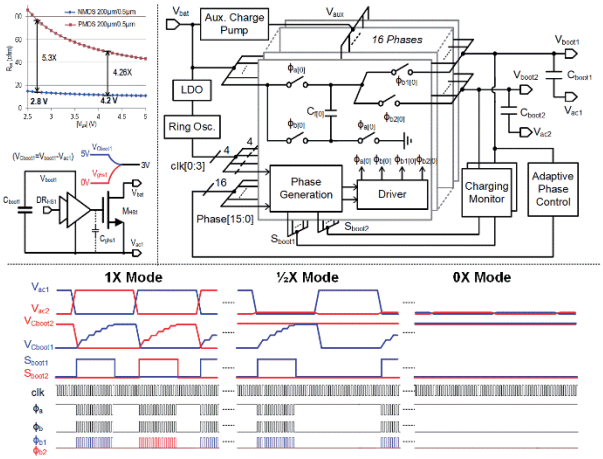

Fig. 4 Block diagram of the on-chip bootstrapping technique and its working principle [8].

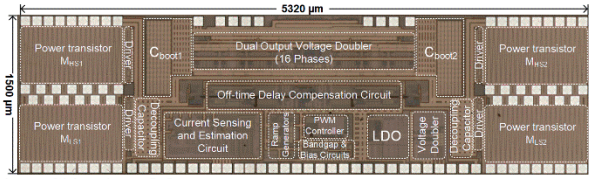

Fig. 5 Chip photo [8].

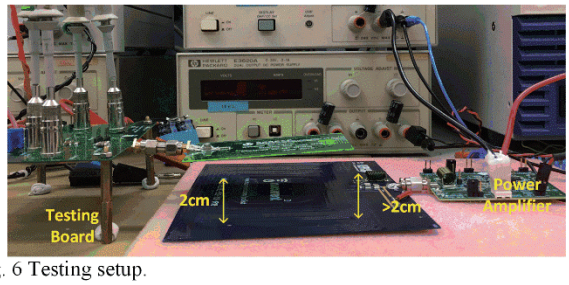

Fig. 6 Testing setup.

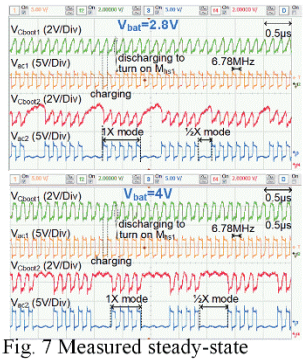

Fig. 7 Measured steady-state waveforms [8].

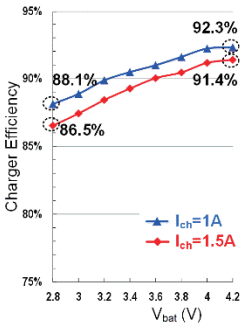

Fig. 8 Measured efficiencies [8].

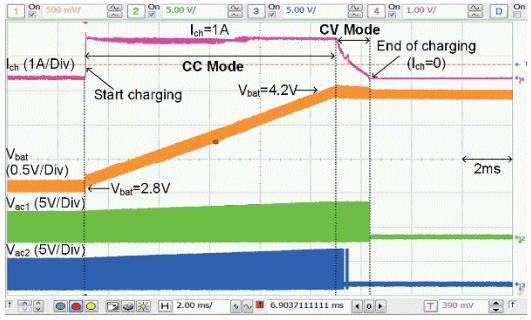

Fig. 9 Measured CC-CV charging profile [8].

TABLE I PERFORMANCE COMPARISON WITH PREVIOUSLY WORKS [8]

	ISSCC 2016 [2]	ISSCC 2017 [5]	ISSCC 2018 [3]	ISSCC 2018 [6]	**This work [8]**
Technology	0.18 μm BCD	0.35 μm CMOS	0.35 μm CMOS	65nm CMOS	**0.35 μm CMOS**
Topology	Rectifier+Buck + Linear charger	Rectifier	Rectifier	Rectifier+ Charge pump	**R³ Rectifier**
Frequency	6.78MHz	6.78MHz	6.78MHz	13.56MHz	**6.78MHz**
Maximum I_{ch}/P_{out}	0.5A/2.5W	0.39A/1.65W	0.6A/2.7W	NA/0.0092W	**1.5A/6.3W**
Charger Efficiency	84% (w/o linear charger)	91.5%	NA	75.4%	**92.3%**
Chip Area	5.83mm²	3.9mm²	3.92mm²	5.11mm²	**8mm²**
Off-chip Components	1 inductor, 3 capacitors	1 capacitor	1 capacitor	NA	**1 capacitor**
Power Stages	3	1	1	2	**1**
CC-CV Charging	Yes	No	No	No	**Yes**