

A 28GHz CMOS Differential Bi-Directional Amplifier for 5G NR

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Abstract - A 28GHz differential bi-directional amplifier in a standard 65nm CMOS process is presented. This work is realized based on the neutralized bi-directional core together with the fully shared inter-stage matching networks. The core chip area is only 0.11mm². At 28GHz, a 15.1-dBm saturation output power and a 4.2-dB noise figure are realized for PA mode and LNA mode, respectively. The DC power consumptions for PA mode and LNA mode are 149mW and 31mW, respectively, under 1-V DC supply.

I. INTRODUCTION

High-speed internet access is an inevitable trend for future network development. By taking advantage of the extensively available bandwidth at millimeter-wave spectrum, the 5G NR n257 band (26.5GHz-29.5GHz) promises an improved data rate on the order of 10Gb/s. However, the free-space-path-loss drastically increases for 28GHz when compared with the sub 6-GHz bands. A larger array size will be mandatory to keep the communication distance. By sharing the antenna and even inter-stage matching networks, the bi-directional operation narrows the transceiver element area, as reported in [1-3]. This is an attractive solution to make the phased-array cost down. Furthermore, a high-output-power PA is also desired to compensate for the propagation loss and relieve the requirement of the system link budget. The differential structure is suitable for PA design and also minimizes the second harmonics. Nowadays, some improvements have been implemented with cross-coupled capacitors [4] and dummy transistors [5] to improve both gain and stability. Derived from these improvements, a differential bi-directional amplifier in a standard 65nm CMOS technology is presented with a core chip area of only 0.11mm².

II. PROPOSED BI-DIRECTIONAL AMPLIFIER DESIGN

Fig. 1 illustrates the proposed 2-stage differential bi-directional amplifier circuit topology with the mode control table. Different from the conventional bi-directional operation based on the RF TRX switch, the TRX mode selection in this work realized by switching the bias voltage occupies a smaller chip area. Also, the inter-stage matching networks are completely shared to further reduce the chip area. The driver stage design is shown in Fig. 2(a). The RX transistor pair (M3 and M4) is selected with the same size as the TX transistor pair (M1 and M2). The two pairs of transistors with opposite directions are connected in a cross-coupling manner. Fig. 2(c) and Fig. 2(d) illustrate the detailed driver stage operation mode. When it operates in TX mode, the TX transistor pair is activated, while the RX transistor pair is shut down, and vice versa. The activated transistor pair's C_{gd} can be neutralized by the off-state transistor pair. Thus, higher gain and better reverse isolation can be achieved. For the PA-LNA stage

shown in Fig. 2(b), a smaller transistor size is suitable for LNA because it contributes less parasitic effect and consumes less DC power; on the contrary, PA demands a large transistor with adequate power capacity. The different PA-LNA transistor size will cause C_{gd} imbalance, which can be compensated by adding an extra capacitor. The TX-mode and RX-mode of the PA-LNA stage are given in Fig. 2(e) and Fig. 2(f), respectively. As for the manner of antenna sharing, the matching points for PA and LNA are quite different; moreover, a balun is necessary to convert the differential connection to the single-ended antenna port. Compared with the 1:2 balun that matches 50Ohm single-ended to 25Ohm in differential, the 1:1 balun is chosen, because it has a higher self-resonant frequency, better Q and coupling efficiency. A switching transistor and a large shunt capacitor C_M are utilized to form the switchable matching network together with this balun, as shown in Fig. 3. By switching the on-off state of VGSW, the matching points can be closer to the required impedances for PA and LNA.

III. MEASUREMENT RESULTS AND CONCLUSION

The proposed 28GHz bi-directional amplifier is fabricated in a standard 65nm CMOS process as part of the bi-directional beamformer. The chip microphotograph is given in Fig. 4. The neutralized bi-directional technique is utilized to improve reverse isolation and gain performance. The bi-directional amplifier only costs 0.11-mm² core chip area by sharing the inter-stage matching network and removing the traditional switches for TRX mode selection. The measured results of this work as part of the beamformer are shown in Fig. 5. At 28GHz, a 15.1-dBm saturation output power and a 4.2-dB noise figure are realized for TX mode and RX mode, respectively. The in-band noise figure is lower than 6dB. Table I demonstrates the performance comparison table. To conclude, this work presents a high output power in TX mode and a reasonable low noise figure in RX mode. The core chip area is greatly minimized by the bi-directional technique. This work is meaningful to support the 5G applications with relatively low cost.

ACKNOWLEDGEMENTS

This work is partially supported by the MIC, SCOPE #175003017, STAR, and VDEC in collaboration with Cadence Design Systems, Inc., Mentor Graphics, Inc., and Keysight Technologies Japan, Ltd.

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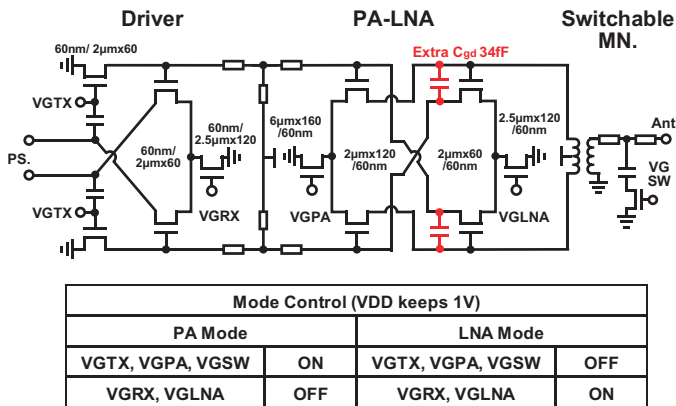


Fig. 1. Proposed 2-stage differential bi-directional amplifier topology and mode control table.

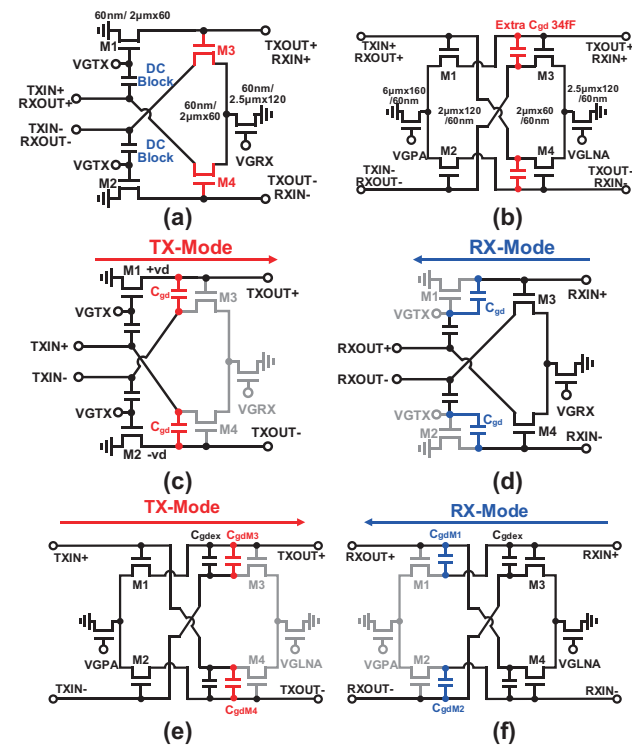


Fig. 2. Circuit schematic of (a) driver stage core, (b) PA-LNA stage core, (c) driver stage in TX mode, (d) driver stage in RX mode, (e) PA-LNA stage in TX mode, and (f) PA-LNA stage in RX mode.

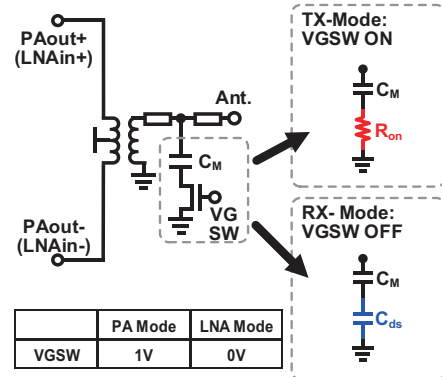


Fig. 3. Switchable matching network and operation mode.

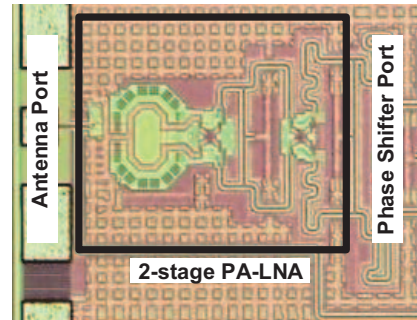


Fig. 4. Microphotograph of the proposed 2-stage differential bi-directional amplifier.

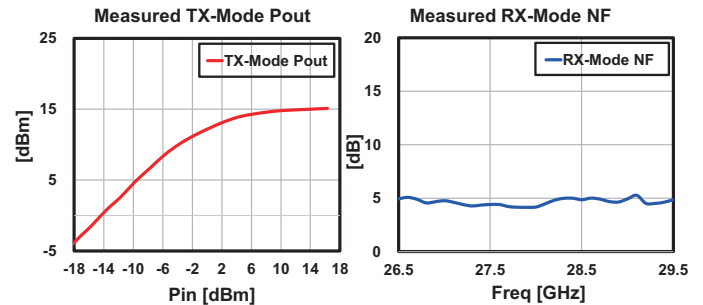


Fig. 5. Measured results of (a) TX-mode output power and (b) RX-mode noise figure.

TABLE I
Performance comparison table.

	ISSCC2017 [6]	RFIC2017 [7]	TMTT2013 [1]	MWCL2018 [3]	This work
Process	0.13μm SiGe BiCMOS	28nm LP CMOS	0.13μm CMOS	0.13μm SiGe BiCMOS	65nm CMOS
Carrier Frequency	28GHz	25.8~28.0GHz	8.5~10.5GHz	28GHz	28GHz
Topology	Individual TRX System	Individual TRX System	Single-ended Cascade Bi-directional Amplifier	Differential Bi-directional Amplifier	Differential Bi-directional Amplifier
TX/PA Psat	16.4dBm	10.5dBm	11.2dBm	-	15.1dBm
TX/PA OP1dB	14.0dBm	9.5dBm	7.4dBm	7.5dBm	11.3dBm
RX/LNA Noise Figure	6.0dB	5.7dB	6.1dB	3.9dB	4.2dB
Core Chip Area	*1.03mm ²	*0.26mm ²	*0.1mm ²	*0.28mm ²	0.11mm ²

*Estimated value