A Quantity Evaluation and Reconfiguration Mechanism for Signal- and Power-Interconnections in 3D-Stacking System

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ABSTRACT

Due to the high integration required for system application, the three-dimensional chip may resolve this requirement. The three-dimensional vertically stacking (3D-stacking) systems have been proposed to satisfy these requirements. However, the 3D-stacking system contains several design risks from its long layer interconnections. For a 3D-stacking system, it is difficult to identify where the numerous power and signal-interconnection are open-, shorted-fault, or resistive-short has accrued. Therefore, solving these interconnection problems is necessary. A feasible interconnection quality-evaluation, fault-diagnosis, and connection-reconfigurable mechanism are proposed. The proposed interconnection-measurement-recovery (IMR) mechanism will make it easy to find interconnection faults and make recovery in 3D-Stacking systems. The proposed IMR can detect interconnection open, short, bridge and resistive defects with the path-reroute mechanism. Future more, the signal transmission quality can be measured. This measurement provides to monitor signal propagation in pico-second accuracy. IMR has less extra area and power consumption overhead. The feasibilities of the proposed mechanism have been justified by 2D-chip and 3D-stacking MorPack both systems.

Keywords-Interconnection, 3D stack system, 3D-IC

I. 3D-STACKING SYSTEM DESIGN

A three-dimensional integrated circuit (3D-IC) is inadequate for the current complex system. Due to the high design costs and extensive design efforts, TSV stacking technology is not broadly adopted. Some modified 3D-IC design technologies are proposed, e.g., Samsung's 2.5-D stacked DRAM dice with TSVs and microbumps on a system-in-package. The true challenge is 3D-stacking across tens of thousands of TSVs on millions of chips.

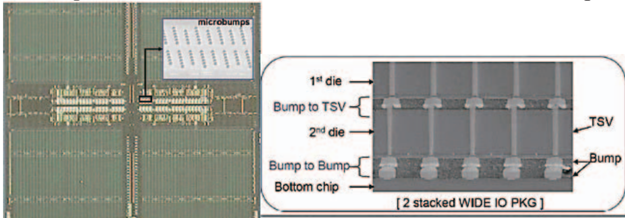


Fig. 1. Samsung's almost-3-D chips 1-Gbit mobile DRAM.

Due to the high design costs and extensive design efforts, the 3D TSV technology is not adopted for designing WPE. The proposed 3D heterogeneous integration system platform- Morphing Package (MorPack) has implemented by Taiwan Semiconductor Research Institute (TSRI), as shown in Figure 2. MorPack is a feasible low-cost 3D package designed a complex system, which has been proposed in [1]. This design technique is utilized to reduce the system's form-factor and power-consumption. The interconnections are within the PCB substrates that belong to each layer. All interconnections are formed by the Ball Grid Array.

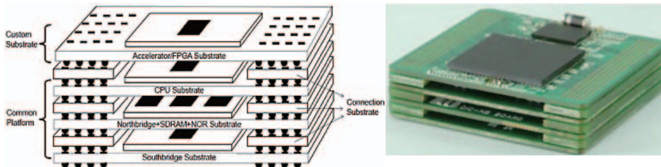


Fig. 2. The MorPack 3D-stacking system.

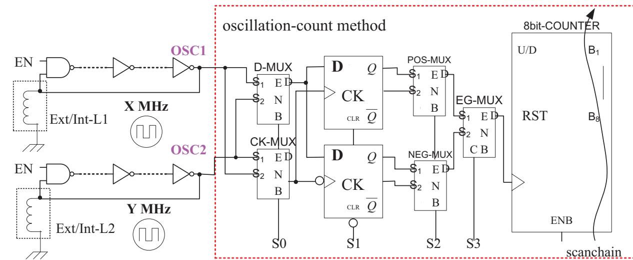
In 3D-stacking system, the multiple supply voltage (Vdd), ground (Vss), and body bias (Vth) turning techniques are applied to the core and IO interface circuits. This will lead to complicated power source track distribution design within the package.

As the interconnections need to be evaluated by signal transmission qualities, e.g. impedance matching, working frequency, and signal integrity related issues. The conventional researches have not to solve these problems.

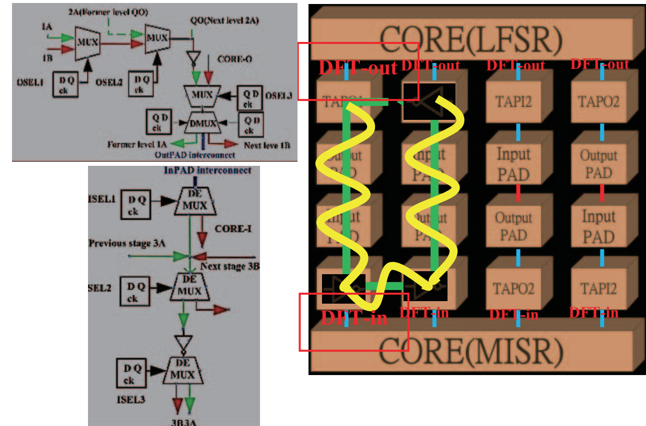
The proposed interconnection-measurement-recovery (IMR) mechanism is a test/measurement and fault-tolerance mechanisms are built within the input-output PADs. An oscillation ring test/measurement methodology is proposed. The generic interconnection's faults (open, short and bridge faults) and signal's transmission quality (e.g. delay-fault) are covered. Future more, the interconnection reconfigurable functionality has been included.

II. THE INTERCONNECTION MEASUREMENT AND RECONFIGURABLE MECHANISM BY DFT CIRCUITS

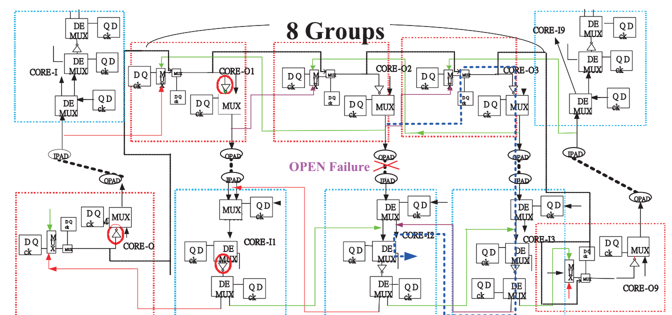
Fig. 3(a) shows the first proposed method of oscillation-count (OC) is for the quick screen the failure interconnection. The interconnection can be evaluated from one-by-one connection; one out-PAD connects to one input-PAD. Figure 3 shows two types of DFT circuities. The ring-oscillation path is constructed from in/out PAD's DFT circuitry. The DFT-In and DFT-Out circuits are used with the PAD connected as a circular ring. The ring than run-on circular-oscillation test/measurement can verify the connected devices within the ring. The IMR mechanism supports faulty interconnection re-routing. This means that the faulty link can be bypassed and reconnect to a good link, allowing all interconnections are well performed. This process is executed using the scan chain to select re-routing paths.



(a) The proposed oscillation count method of IMR.



(b) DFT-In/Out (c) Built Oscillation-rings (OSC1,OSC2) by DFT



(e) Interconnection reconfigurable (blue dash-line for open failure)
Fig. 3. The interconnection with DFT in PAD circuits.

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Figure 4(a) shows transmission-time measurement for accurately measuring the signal transmission quality of the interconnection for high-quality interconnection, e.g. clock signal. The comparison is obtained from two oscillation-rings, OSC1, and OSC2 that obtained from Fig. 3. The proposed circuit structure of the Built-in Delay Measurement (BISM) mechanism. The VDL (Vernier Delay Line) is a simple and high-resolution circuit delay time measurement structure adopted in BISM. The BISM circuit Coarse-Block (CB) is 130ps accuracy as shown in Fig. 4(b).

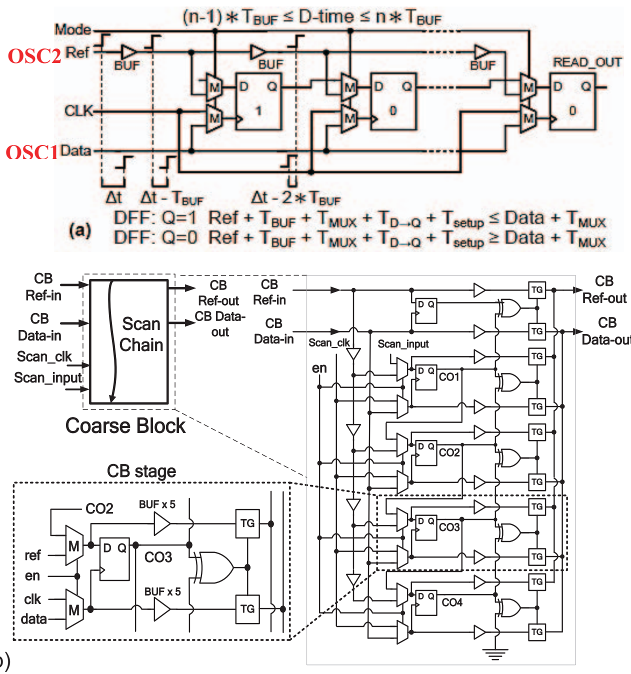


Fig. 4. The high-accurate interconnection quantity measurement.

As these power-link occupy a large number of interconnections in the 3D-stacking design. Not only the interconnection short/open faults are considered, but also the interconnection is shorted with power interconnection. Figure 5 shows the circuit design of RetFF, RetFF power can be a short-time turn-off and logic state can be preserved for the short-time duration. The RetFF is used in the powerless state can detect interconnection fault comes from power.

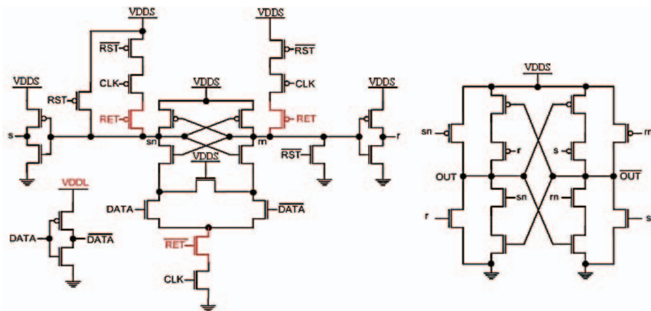
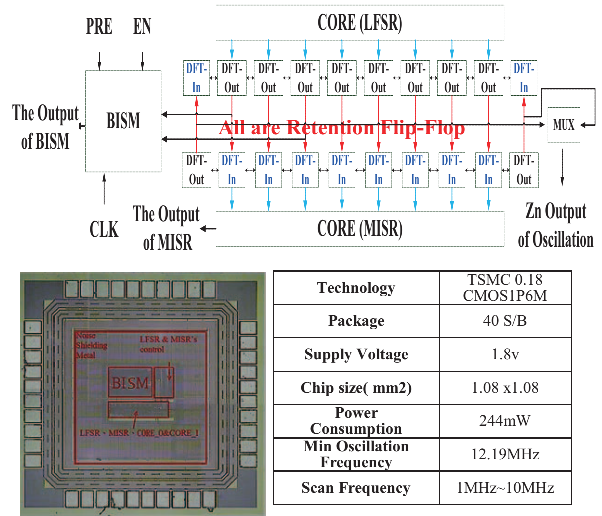


Fig. 5. The retention Flip-Flop (RetFF) in LFSR, MISR circuits.

IV. Test Chip Design and 2D/3D-Stacking System Validations

A test chip is designed for evaluating the efficiency of IMR method, the circuit structure is shown in Figure 6. Both the 2D and 3D-stacking systems are used to verify the proposed mechanisms. The 2D system is constructed by four single chips (Figure 7). The 3D-stacking system is built by stacking-microbump as a MorPack system. In Figure 8, the red-box is the output from the MISR circuit. The case of open-fault can be detected and located. The fault also has found from X-ray shown in Fig. 9. Table 1 shows a comparison with the existent technique. IMR is applicable for quantizing, multiple faults and located faults.



Technology	TSMC 0.18 CMOS1P6M
Package	40 S/B
Supply Voltage	1.8v
Chip size(mm2)	1.08 x1.08
Power Consumption	244mW
Min Oscillation Frequency	12.19MHz
Scan Frequency	1MHz~10MHz

Fig. 6. shows the single test chip and specifications.

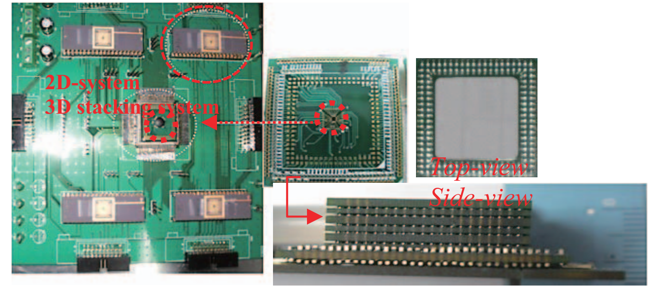


Fig. 7. 2D system and mounted to a 3D-stacking system.

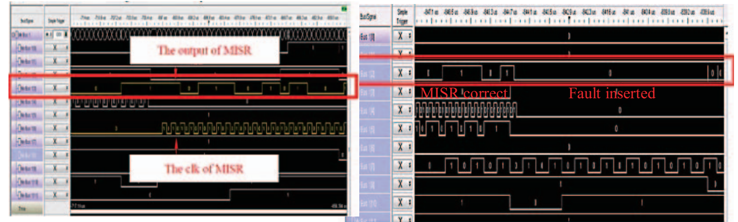


Fig. 8. The validation under the case of testing open fault

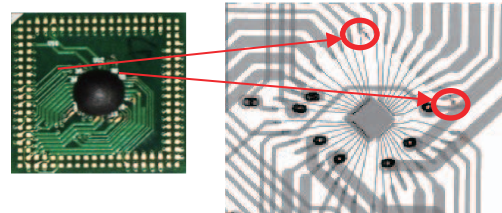


Fig. 9. The fault found in MorPack with X-ray diagnosis.

Table 1. The comparisons of the proposed 3D-stacking mechanism

Design	Ref. [2]	Bound-Scan	Proposed
short & open faults	Yes	Yes	Yes
Resistant fault	No	No	Yes
Fault Tolerance	No	No	Yes
Controllability	Complex	Complex	Easy
Route Debugging	Yes	Partial	Yes
Chip verification	No	Yes	Yes

V. Conclusion

This paper proposes a feasible interconnection test/measurement method with a reconfigurable scheme to detect open, short and resistive bridges in 3D-Stacking systems.

[1] C.-M. Huang, C.-M. Wu, C.-C.Yang, W.-D. Chien and C.L. Wey, “A Package Carrier with a Custom Interface”, US patent: US 7,755,177 B2.

[2] K. Arabi and B. Kaminska, "Oscillation-test methodology for low-cost testing of active analog filters," in *IEEE Transactions on Instrumentation and Measurement*, Aug. 1999.